In the claims:

Claim 1. Cancelled.

2. (Previously presented) A DRAM circuit comprising a plurality of aligned sense amplifiers,

bit line pairs connected to the plurality of sense amplifiers, respectively, and

memory cells connected respectively to the bit lines constituting the bit line pairs, wherein

the bit line pairs and the memory cells are alternately arranged on a right side (upper side) and a left side (lower side) of the sense amplifiers per N (N: natural number) aligned sense amplifiers, wherein there cross two bit lines constituting the bit line pair arranged on one side of a right side (upper side) and a left side (lower side) of the sense amplifier, and a space between the bit lines widens or narrows from the cross.

3. (Original) The DRAM circuit according to claim 2, wherein, further, two bit lines constituting the bit line pair, which is arranged on the other side of the one right side (upper side) or left side (lower side) of the sense amplifier, do not cross, and a space therebetween widens or narrows on the way.

Claims 4. and 5. Cancelled

6. (Original) The DRAM circuit according to claim 3, wherein the bit line pairs comprise a bit line configuration in a multiple twisted bit line (MTBL) method.

Claims 7. and 8. Cancelled.

9. (Previously presented) A DRAM circuit comprising a plurality of sense amplifiers SA (J, K) arranged in Q lines each containing the P sense amplifiers,

bit line pairs connected to the plurality of sense amplifiers SA (J, K), respectively, and

memory cells connected respectively to the bit lines constituting the bit line pairs, wherein

the sense amplifier SA (J, K) is connected to each of the bit line pairs arranged between the sense amplifier SA (J, K) and a sense amplifier SA (J, K-1) in one next line;

a sense amplifier SA (J+1, K) is connected to the bit line pairs arranged between the sense amplifier SA (J+1, K) and a sense amplifier SA (J+1, K+1) in another next line;

a sense amplifier SA (J--2 3, K) is connected to each of the bit line pairs arranged between the sense amplifier SA (J+2 3, K) and a sense amplifier SA (J+2, K-1) in one next line; and

P and Q are both integers of more than 3, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q, wherein two bit lines constituting the bit line pair, which is arranged in one space between the sense amplifier SA (J, K) and the sense amplifier SA (J, K-1) in the next line, cross, and from the cross, a space between the two bit lines widens or narrows.

10. (Previously presented) A DRAM circuit comprising a plurality of sense amplifiers SA (J, K) arranged in Q lines each containing the P sense amplifiers,

bit line pairs connected to the plurality of sense amplifiers SA (J, K), respectively, and

memory cells connected respectively to the bit lines constituting the bit line pairs, wherein

the sense amplifier SA (J, K) is connected to each of the bit line pairs arranged between the sense amplifier SA (J, K) and a sense amplifier SA (J, K-1) in one next line or a sense amplifier SA (J, K+1) in the other next line;

a sense amplifier SA (J+1, K) is connected to the bit line pairs arranged between the sense amplifier SA (J+1, K) and a sense amplifier SA (J+1, K+1) in one next line or a sense amplifier SA (J+1, K-1) in the other next line;

a sense amplifier SA (J−3, K) is connected to each of the bit line pairs arranged between the sense amplifier SA (J+3, K) and a sense amplifier SA (J+2, K-1) in one next line or a sense amplifier SA (J+2, K+1) in the other next line; and

P and Q are both integers of more than 3, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q, wherein two bit lines constituting the bit line pair, which is arranged in one space between the sense amplifier SA (J, K) and the sense amplifier SA (J, K+1) or SA (J, K-1) in the next line, cross, and from the cross, a space between the two bit lines widens or narrows and wherein, further, two bit lines constituting the bit line pair, which is arranged in a space opposite to the one space between the sense amplifier SA (J, K) and the sense amplifier SA (J, K+1) or SA (J, K-1) in the next line, do not cross, and a space therebetween widens or narrows on the way.

Claims 11. and 12. Cancelled.

13. (Original) The DRAM circuit according to claim 10, wherein the bit line pairs comprise a bit line configuration in a multiple twisted bit line (MTBL) method.

Claim 14. Cancelled.

15. (Original) An operation method of a DRAM circuit comprising a plurality of aligned sense amplifiers,

bit line pairs connected to the plurality of sense amplifiers, respectively, and

memory cells connected respectively to the bit lines constituting the bit line pairs, wherein

the bit line pairs and memory cells are alternately arranged on a right side (upper side) and a left side (lower side) of the sense amplifiers per N (N: natural number) aligned sense amplifiers,

the method comprising a step of activating the plurality of sense amplifiers connected to the bit line pairs and memory cells arranged on the right side (upper side) of the sense amplifiers, and the plurality of sense amplifiers connected to the bit line pairs and memory cells arranged on the left side (lower side) of the sense amplifiers at different timing, when data is read.

16. (Original) An operation method of a DRAM circuit comprising:

a plurality of sense amplifiers arranged in Q lines each containing the P sense amplifiers;

bit line pairs connected to the plurality of sense amplifiers, respectively; and

memory cells connected respectively to the bit lines constituting the bit line pairs,

wherein the bit line pairs and the memory cells are arranged every N (N: natural number) aligned sense amplifiers in the Q lines, alternately on a right side (upper side) and a left side (lower side) of the sense amplifiers, and P and Q are both integers of more than 3, and N is an arbitrary integer of more than 1 and less than (P/3);

the method comprising a step of activating the plurality of sense amplifiers connected to the bit line pairs and memory cells arranged on the right side (upper side) of the sense amplifiers, and the plurality of sense amplifiers connected to the bit line pairs and memory cells arranged on the left side (lower side) of the sense amplifiers at different timing, when data is read.

17. (Original) An operation method of a DRAM circuit comprising:

a plurality of sense amplifiers SA (J, K) arranged in Q lines each containing the P sense amplifiers;

bit line pairs connected to the plurality of sense amplifiers SA (J, K), respectively; and

memory cells connected respectively to the bit lines constituting the bit line pairs,

wherein the sense amplifier SA (J, K) is connected to each of the bit line pairs arranged between the sense amplifier SA (J, K) and a sense amplifier SA (J, K-1) in one next line or a sense amplifier SA (J, K+1) in the other next line;

a sense amplifier SA (J+1, K) is connected to the bit line pair arranged between the sense amplifier SA (J+1, K) and a sense amplifier SA (J+1, K+1) in one next line or a sense amplifier SA (J+1, K-1) in the other next line;

a sense amplifier SA (J+3, K) is connected to the bit line pair arranged between the sense amplifier SA (J+3, K) and a sense amplifier SA (J+2, K-1) in one next line or a sense amplifier SA (J+2, K+1) in the other next line; and

P and Q are both integers of more than 3, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q;

the method comprising a step of activating the sense amplifier SA (J+1, K) at timing different from the sense amplifier SA (J, K) and the sense amplifier SA (J+3, K), when data is read.

18. (Original) An operation method of a DRAM circuit comprising:

a plurality of sense amplifiers SA (J, K) arranged in Q lines each containing the P sense amplifiers;

bit line pairs connected to the plurality of sense amplifiers SA (J, K), respectively; and

memory cells connected respectively to the bit lines constituting the bit line pairs,

wherein sense amplifier SA (J, K) and a sense amplifier SA (J+1, K) are each connected to each of the bit line pairs arranged between a sense amplifier SA (J, K-1) in one next line and a sense amplifier SA (J+1, K-1) or between a sense amplifier SA (J, K+1) in the other next line and a sense amplifier SA (J+1, K+1);

a sense amplifier SA (J+2, K) and a sense amplifier SA (J+3, K) are each connected to the bit line pairs arranged between a sense amplifier SA (J+2, K+1) in one next line and a sense amplifier SA (J+3, K+1) or between a sense amplifier SA (J+2, K-1) in the other next line and a sense amplifier SA (J+3, K-1);

a sense amplifier SA (J+4, K) and a sense amplifier SA (J+5, K) are each connected to each of the bit line pairs arranged between a sense amplifier SA (J+4, K-1) in one next line and a sense amplifier SA (J+5, K-1) or between a sense amplifier SA (J+4, K+1) in the other next line and a sense amplifier SA (J+4, K+1); and

P and Q are both integers of more than 6, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q;

the method comprising a step of activating the sense amplifier SA (J, K), the sense amplifier SA (J+1, K), the sense amplifier SA (J+4, K) and the sense amplifier SA (J+5, K) at timing different from the sense amplifier SA (J+2, K) and the sense amplifier SA (J+3, K), when data is read.

Claims 19. and 20. Cancelled.